

This file lists the names defined in CodeWarrior C (version 6.1) for the registers in the MC68HC908JL16.

This information is taken from the file "mc68hc908jl16.h" which is in the "C:\Program Files\Freescale\CW08 V5.1\lib\hc08c\device\include" folder.

NOTE: Not all names apply to all versions of the JL16 since some pins are not available on all packages.

These names can be used in assignment statements to read and write the contents of the registers.

```
PTA = 0x25;
x = DDRA;
```

Some of the timer registers are the upper and lower parts of a 16-bit register. The combined 16-bit register can be accessed with a single statement.

```
T1MOD = 0x2345;
```

This is equivalent to

```
T1MODH = 0x23;
T1MODL = 0x45;
```

The individual bits in the registers can also be read and written by using the names defined below for the bits.

```
PTB_PTB7 = 1;
if (PTA_PTA2) { .... }
```

Some registers have groups of two or more bits that are parts of a single quantity. These can be accessed with a single statement.

```
T1SC_PS = 5;
```

This is equivalent to

```
T1SC_PS2 = 1;
T1SC_PS1 = 0;
T1SC_PS0 = 1;
```

Note that assignments to register locations that write less than the full eight bits will generate code that first reads the register, modifies the bits as needed, and then writes all eight bits back.

Port A Data Register (0x0000)	PTA
PTA_PTA7	bit 7 - Port A Data Bit 7
PTA_PTA6	bit 6 - Port A Data Bit 6
PTA_PTA5	bit 5 - Port A Data Bit 5
PTA_PTA4	bit 4 - Port A Data Bit 4
PTA_PTA3	bit 3 - Port A Data Bit 3
PTA_PTA2	bit 2 - Port A Data Bit 2
PTA_PTA1	bit 1 - Port A Data Bit 1
PTA_PTA0	bit 0 - Port A Data Bit 0

Port B Data Register (0x0001)	PTB
PTB_PTB7	bit 7 - Port B Data Bit 7
PTB_PTB6	bit 6 - Port B Data Bit 6
PTB_PTB5	bit 5 - Port B Data Bit 5
PTB_PTB4	bit 4 - Port B Data Bit 4
PTB_PTB3	bit 3 - Port B Data Bit 3
PTB_PTB2	bit 2 - Port B Data Bit 2

PTB_PTB1 bit 1 - Port B Data Bit 1
 PTB_PTB0 bit 0 - Port B Data Bit 0

Port D Data Register (0x0003) PTD
 PTD_PTD7 bit 7 - Port D Data Bit 7
 PTD_PTD6 bit 6 - Port D Data Bit 6
 PTD_PTD5 bit 5 - Port D Data Bit 5
 PTD_PTD4 bit 4 - Port D Data Bit 4
 PTD_PTD3 bit 3 - Port D Data Bit 3
 PTD_PTD2 bit 2 - Port D Data Bit 2
 PTD_PTD1 bit 1 - Port D Data Bit 1
 PTD_PTD0 bit 0 - Port D Data Bit 0

Data Direction Register A (0x0004) DDRA
 DDRA_DDRA7 bit 7 - Data Direction Register A Bit 7
 DDRA_DDRA6 bit 6 - Data Direction Register A Bit 6
 DDRA_DDRA5 bit 5 - Data Direction Register A Bit 5
 DDRA_DDRA4 bit 4 - Data Direction Register A Bit 4
 DDRA_DDRA3 bit 3 - Data Direction Register A Bit 3
 DDRA_DDRA2 bit 2 - Data Direction Register A Bit 2
 DDRA_DDRA1 bit 1 - Data Direction Register A Bit 1
 DDRA_DDRA0 bit 0 - Data Direction Register A Bit 0

Data Direction Register B (0x0005) DDRB
 DDRB_DDRB7 bit 7 - Data Direction Register B Bit 7
 DDRB_DDRB6 bit 6 - Data Direction Register B Bit 6
 DDRB_DDRB5 bit 5 - Data Direction Register B Bit 5
 DDRB_DDRB4 bit 4 - Data Direction Register B Bit 4
 DDRB_DDRB3 bit 3 - Data Direction Register B Bit 3
 DDRB_DDRB2 bit 2 - Data Direction Register B Bit 2
 DDRB_DDRB1 bit 1 - Data Direction Register B Bit 1
 DDRB_DDRB0 bit 0 - Data Direction Register B Bit 0

Data Direction Register D (0x0007) DDRD
 DDRD_DDRD7 bit 7 - Data Direction Register D Bit 7
 DDRD_DDRD6 bit 6 - Data Direction Register D Bit 6
 DDRD_DDRD5 bit 5 - Data Direction Register D Bit 5
 DDRD_DDRD4 bit 4 - Data Direction Register D Bit 4
 DDRD_DDRD3 bit 3 - Data Direction Register D Bit 3
 DDRD_DDRD2 bit 2 - Data Direction Register D Bit 2
 DDRD_DDRD1 bit 1 - Data Direction Register D Bit 1
 DDRD_DDRD0 bit 0 - Data Direction Register D Bit 0

Port E Data Register (0x0008) PTE
 PTE_PTE1 bit 1 - Port E Data Bit 1
 PTE_PTE0 bit 0 - Port E Data Bit 0

Port D Control Register (0x000A) PDCR
 PDCR_SLOWD7 bit 3 - Slow Edge Enable bit 7, port D
 PDCR_SLOWD6 bit 2 - Slow Edge Enable bit 6, port D
 PDCR_PTDPU7 bit 1 - Pull-Up Enable bit 7, port D
 PDCR_PTDPU6 bit 0 - Pull-Up Enable bit 6, port D

 PDCR_SLOWD bits 2-3 - Slow Edge Enable, port D
 PDCR_PTDPU bits 0-1 - Pull-Up Enable, port D

Data Direction Register E (0x000C) DDRE
 DDRE_DDRE1 bit 1 - Data Direction Register E Bit 1
 DDRE_DDRE0 bit 0 - Data Direction Register E Bit 0

Port A Input Pull-Up Enable (0x000D) PTAPUE
 PTAPUE_PTA6EN bit 7 - Enable PTA6 on OSC2, Port A

PTAPUE_PTAPUE6	bit 6 - Pull-Up Enable bit 6, Port A
PTAPUE_PTAPUE5	bit 5 - Pull-Up Enable bit 5, Port A
PTAPUE_PTAPUE4	bit 4 - Pull-Up Enable bit 4, Port A
PTAPUE_PTAPUE3	bit 3 - Pull-Up Enable bit 3, Port A
PTAPUE_PTAPUE2	bit 2 - Pull-Up Enable bit 2, Port A
PTAPUE_PTAPUE1	bit 1 - Pull-Up Enable bit 1, Port A
PTAPUE_PTAPUE0	bit 0 - Pull-Up Enable bit 0, Port A
PTAPUE_PTAPUE	bits 0-6 - Pull-Up Enable, Port A

Input Pull-Up Enable Register (0x000E) PTA7PUE
 PTA7PUE_PTAPUE7 bit 7 - Pull-Up Enable bit 7, Port A

SCI Control Register 1 (0x0013) SCC1

SCC1_LOOPS	bit 7 - Loop Mode Select Bit
SCC1_ENSCI	bit 6 - Enable SCI Bit
SCC1_TXINV	bit 5 - Transmit Inversion Bit
SCC1_M	bit 4 - Mode (Character Length) Bit
SCC1_WAKE	bit 3 - Wakeup Condition Bit
SCC1_ILTY	bit 2 - Idle Line Type Bit
SCC1_PEN	bit 1 - Parity Enable Bit
SCC1_PTY	bit 0 - Parity Bit

SCI Control Register 2 (0x0014) SCC2

SCC2_SCTIE	bit 7 - SCI Transmit Interrupt Enable Bit
SCC2_TCIE	bit 6 - Transmission Complete Interrupt Enable Bit
SCC2_SCRIE	bit 5 - SCI Receive Interrupt Enable Bit
SCC2_ILIE	bit 4 - Idle Line Interrupt Enable Bit
SCC2_TE	bit 3 - Transmitter Enable Bit
SCC2_RE	bit 2 - Receiver Enable Bit
SCC2_RWU	bit 1 - Receiver Wakeup Bit
SCC2_SBK	bit 0 - Send Break Bit

SCI Control Register 3 (0x0015) SCC3

SCC3_R8	bit 7 - Received Bit 8
SCC3_T8	bit 6 - Transmitted Bit 8
SCC3_ORIE	bit 3 - Receiver Overrun Interrupt Enable Bit
SCC3_NEIE	bit 2 - Receiver Noise Error Interrupt Enable Bit
SCC3_FEIE	bit 1 - Receiver Framing Error Interrupt Enable Bit
SCC3_PEIE	bit 0 - Receiver Parity Error Interrupt Enable Bit

SCI Status Register 1 (0x0016) SCS1

SCS1_SCTE	bit 7 - SCI Transmitter Empty Bit
SCS1_TC	bit 6 - Transmission Complete Bit
SCS1_SCRF	bit 5 - SCI Receiver Full Bit
SCS1_IDLE	bit 4 - Receiver Idle Bit
SCS1_OR	bit 3 - Receiver Overrun Bit
SCS1_NF	bit 2 - Receiver Noise Flag Bit
SCS1_FE	bit 1 - Receiver Framing Error Bit
SCS1_PE	bit 0 - Receiver Parity Error Bit

SCI Status Register 2 (0x0017) SCS2

SCS2_BKF	bit 1 - Break Flag Bit
SCS2_RPF	bit 0 - Reception in Progress Flag Bit

SCI Data Register (0x0018) SCDR

SCDR_R7_T7	bit 7 - Receive/Transmit Data Bit 7
SCDR_R6_T6	bit 6 - Receive/Transmit Data Bit 6
SCDR_R5_T5	bit 5 - Receive/Transmit Data Bit 5
SCDR_R4_T4	bit 4 - Receive/Transmit Data Bit 4
SCDR_R3_T3	bit 3 - Receive/Transmit Data Bit 3
SCDR_R2_T2	bit 2 - Receive/Transmit Data Bit 2

SCDR_R1_T1 bit 1 - Receive/Transmit Data Bit 1
 SCDR_R0_T0 bit 0 - Receive/Transmit Data Bit 0

SCI Baud Rate Register (0x0019) SCBR
 SCBR_SCP1 bit 5 - SCI Baud Rate Prescaler Bit 1
 SCBR_SCP0 bit 4 - SCI Baud Rate Prescaler Bit 0
 SCBR_SCR2 bit 2 - SCI Baud Rate Select Bit 2
 SCBR_SCR1 bit 1 - SCI Baud Rate Select Bit 1
 SCBR_SCR0 bit 0 - SCI Baud Rate Select Bit 0

 SCBR_SCP bits 4-5 - SCI Baud Rate Prescaler
 SCBR_SCR bits 0-2 - SCI Baud Rate Select

Keyboard Status and Control Register (0x001A) KBSCR
 KBSCR_KEYF bit 3 - Keyboard Flag Bit
 KBSCR_ACKK bit 2 - Keyboard Acknowledge Bit
 KBSCR_IMASKK bit 1 - Keyboard Interrupt Mask Bit
 KBSCR_MODEK bit 0 - Keyboard Triggering Sensitivity Bit

Keyboard Interrupt Enable Register (0x001B) KBIER
 KBIER_KBIE7 bit 7 - Keyboard Interrupt Enable Bit 7
 KBIER_KBIE6 bit 6 - Keyboard Interrupt Enable Bit 6
 KBIER_KBIE5 bit 5 - Keyboard Interrupt Enable Bit 5
 KBIER_KBIE4 bit 4 - Keyboard Interrupt Enable Bit 4
 KBIER_KBIE3 bit 3 - Keyboard Interrupt Enable Bit 3
 KBIER_KBIE2 bit 2 - Keyboard Interrupt Enable Bit 2
 KBIER_KBIE1 bit 1 - Keyboard Interrupt Enable Bit 1
 KBIER_KBIE0 bit 0 - Keyboard Interrupt Enable Bit 0

IRQ Status and Control Register (0x001D) INTSCR
 INTSCR_IRQF bit 3 - IRQ Flag
 INTSCR_ACK bit 2 - IRQ Interrupt Request Acknowledge Bit
 INTSCR_IMASK bit 1 - IRQ Interrupt Mask Bit
 INTSCR_MODE bit 0 - IRQ Edge/Level Select Bit

Configuration Register 2 (0x001E) CONFIG2
 CONFIG2_IRQPUD bit 7 - IRQ1 Pin Pull-Up Control Bit
 CONFIG2_LVIT1 bit 4 - Low Voltage Inhibit Trip Voltage Select Bit 1
 CONFIG2_LVIT0 bit 3 - Low Voltage Inhibit Trip Voltage Select Bit 0
 CONFIG2_IICSEL bit 1 - MMIIIC Pin Selection Bit
 CONFIG2_STOP_ICLKDIS bit 0 - Internal oscillator STOP mode disable bit

 CONFIG2_LVIT bits 3-4 - Low Voltage Inhibit Trip Voltage Select

Configuration Register 1 (0x001F) CONFIG1
 CONFIG1_COPRS bit 7 - COP Reset Period Selection Bit
 CONFIG1_LVID bit 4 - Low Voltage Inhibit Disable Bit
 CONFIG1_SSREC bit 2 - Short Stop Recovery Bit
 CONFIG1_STOP bit 1 - STOP Instruction Enable Bit
 CONFIG1_COPD bit 0 - COP Disable Bit

TIM1 Status and Control Register (0x0020) T1SC
 T1SC_TOF bit 7 - TIM1 Overflow Flag Bit
 T1SC_TOIE bit 6 - TIM1 Overflow Interrupt Enable Bit
 T1SC_TSTOP bit 5 - TIM1 Stop Bit
 T1SC_TRST bit 4 - TIM1 Reset Bit
 T1SC_PS2 bit 2 - Prescaler Select Bit 2
 T1SC_PS1 bit 1 - Prescaler Select Bit 1
 T1SC_PS0 bit 0 - Prescaler Select Bit 0

 T1SC_PS bits 0-2 - Prescaler Select

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TIM1 Counter Register (0x0021:0x0022)    T1CNT
TIM1 Counter Register High (0x0021)      T1CNTH
TIM1 Counter Register Low (0x0022)       T1CNTL

TIM1 Counter Modulo Register (0x0023:0x0024)  T1MOD
TIM1 Counter Modulo Register High (0x0023)    T1MODH
TIM1 Counter Modulo Register Low (0x0024)     T1MODL

TIM1 Channel 0 Status and Control Register (0x0025)    T1SC0
  T1SC0_CH0F      bit 7 - Channel 0 Flag Bit
  T1SC0_CH0IE    bit 6 - Channel 0 Interrupt Enable Bit
  T1SC0_MS0B     bit 5 - Mode Select Bit B
  T1SC0_MS0A     bit 4 - Mode Select Bit A
  T1SC0_ELS0B    bit 3 - Edge/Level Select Bit B
  T1SC0_ELS0A    bit 2 - Edge/Level Select Bit A
  T1SC0_TOV0     bit 1 - Toggle-On-Overflow Bit
  T1SC0_CH0MAX   bit 0 - Channel 0 Maximum Duty Cycle Bit

  T1SC0_MS0x     bits 4-5 - Mode Select
  T1SC0_ELS0x    bits 2-3 - Edge/Level Select

TIM1 Channel 0 Register (0x0026:0x0027) T1CH0
TIM1 Channel 0 Register High (0x0026)    T1CH0H
TIM1 Channel 0 Register Low (0x0027)     T1CH0L

TIM1 Channel 1 Status and Control Register (0x0028)    T1SC1
  T1SC1_CH1F      bit 7 - Channel 1 Flag Bit
  T1SC1_CH1IE    bit 6 - Channel 1 Interrupt Enable Bit
  T1SC1_MS1A     bit 4 - Mode Select Bit A
  T1SC1_ELS1B    bit 3 - Edge/Level Select Bit B
  T1SC1_ELS1A    bit 2 - Edge/Level Select Bit A
  T1SC1_TOV1     bit 1 - Toggle-On-Overflow Bit
  T1SC1_CH1MAX   bit 0 - Channel 1 Maximum Duty Cycle Bit

  T1SC1_ELS1x    bits 2-3 - Edge/Level Select

TIM1 Channel 1 Register (0x0029:0x002A) T1CH1
TIM1 Channel 1 Register High (0x0029)    T1CH1H
TIM1 Channel 1 Register Low (0x002A)     T1CH1L

TIM2 Status and Control Register (0x0030)    T2SC
  T2SC_TOF      bit 7 - TIM1 Overflow Flag Bit
  T2SC_TOIE    bit 6 - TIM1 Overflow Interrupt Enable Bit
  T2SC_TSTOP   bit 5 - TIM1 Stop Bit
  T2SC_TRST    bit 4 - TIM1 Reset Bit
  T2SC_PS2     bit 2 - Prescaler Select Bit 2
  T2SC_PS1     bit 1 - Prescaler Select Bit 1
  T2SC_PS0     bit 0 - Prescaler Select Bit 0

  T2SC_PS      bits 0-2 - Prescaler Select

TIM2 Counter Register (0x0031:0x0032)    T2CNT

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TIM2 Counter Register High (0x0031)      T2CNTH
TIM2 Counter Register Low (0x0032)      T2CNTL

TIM2 Counter Modulo Register (0x0033:0x0034)  T2MOD
TIM2 Counter Modulo Register High (0x0033)  T2MODH
TIM2 Counter Modulo Register Low (0x0034)   T2MODL

TIM2 Channel 0 Status and Control Register (0x0035)  T2SC0
T2SC0_CH0F      bit 7 - Channel 0 Flag Bit
T2SC0_CH0IE     bit 6 - Channel 0 Interrupt Enable Bit
T2SC0_MS0B      bit 5 - Mode Select Bit B
T2SC0_MS0A      bit 4 - Mode Select Bit A
T2SC0_ELS0B     bit 3 - Edge/Level Select Bit B
T2SC0_ELS0A     bit 2 - Edge/Level Select Bit A
T2SC0_TOV0      bit 1 - Toggle-On-Overflow Bit
T2SC0_CH0MAX    bit 0 - Channel 0 Maximum Duty Cycle Bit

T2SC0_MS0x      bits 4-5 - Mode Select
T2SC0_ELS0x     bits 2-3 - Edge/Level Select

TIM2 Channel 0 Register (0x0036:0x0037) T2CH0
TIM2 Channel 0 Register High (0x0036)     T2CH0H
TIM2 Channel 0 Register Low (0x0037)      T2CH0L

TIM2 Channel 1 Status and Control Register (0x0038)  T2SC1
T2SC1_CH1F      bit 7 - Channel 1 Flag Bit
T2SC1_CH1IE     bit 6 - Channel 1 Interrupt Enable Bit
T2SC1_MS1A      bit 4 - Mode Select Bit A
T2SC1_ELS1B     bit 3 - Edge/Level Select Bit B
T2SC1_ELS1A     bit 2 - Edge/Level Select Bit A
T2SC1_TOV1      bit 1 - Toggle-On-Overflow Bit
T2SC1_CH1MAX    bit 0 - Channel 1 Maximum Duty Cycle Bit

T2SC0_ELS1x     bits 2-3 - Edge/Level Select

TIM2 Channel 1 Register (0x0039:0x003A) T2CH1
TIM2 Channel 1 Register High (0x0039)     T2CH1H
TIM2 Channel 1 Register Low (0x003A)      T2CH1L

ADC10 Status and Control Register (0x003C)  ADSCR
ADSCR_COCO      bit 7 - Conversions Complete Bit
ADSCR_AIEN      bit 6 - ADC10 Interrupt Enable Bit
ADSCR_ADCO      bit 5 - ADC10 Continuous Conversion Bit
ADSCR_CH4       bit 4 - ADC10 Channel Select Bit 4
ADSCR_CH3       bit 3 - ADC10 Channel Select Bit 3
ADSCR_CH2       bit 2 - ADC10 Channel Select Bit 2
ADSCR_CH1       bit 1 - ADC10 Channel Select Bit 1
ADSCR_CH0       bit 0 - ADC10 Channel Select Bit 0

ADSCR_CH        bits 0-4 - ADC10 Channel Select

ADC10 Data Register (0x003D)              ADR
ADC10 Data Register High (0x003D)        ADRH
ADRH_AD9        bit 1 - ADC10 Data Bit 9
ADRH_AD8        bit 0 - ADC10 Data Bit 8

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ADC10 Data Register Low (0x003E) ADRL

ADRL_AD7	bit 7 - ADC10 Data Bit 7
ADRL_AD6	bit 6 - ADC10 Data Bit 6
ADRL_AD5	bit 5 - ADC10 Data Bit 5
ADRL_AD4	bit 4 - ADC10 Data Bit 4
ADRL_AD3	bit 3 - ADC10 Data Bit 3
ADRL_AD2	bit 2 - ADC10 Data Bit 2
ADRL_AD1	bit 1 - ADC10 Data Bit 1
ADRL_AD0	bit 0 - ADC10 Data Bit 0

ADC10 Input Clock Register (0x003F) ADCLK

ADCLK_ADLPC	bit 7 - ADC10 Low-Power Configuration Bit
ADCLK_ADIV1	bit 6 - ADC Clock Prescaler Bit 1
ADCLK_ADIV0	bit 5 - ADC Clock Prescaler Bit 0
ADCLK_ADICLK	bit 4 - Input Clock Select Bit
ADCLK_MODE1	bit 3 - 10- or 8-Bit or External-Triggered Mode Selection Bit 1
ADCLK_MODE0	bit 2 - 10- or 8-Bit or External-Triggered Mode Selection Bit 0
ADCLK_ADLSMP	bit 1 - Long Sample Time Configuration
ADCLK_ACLKEN	bit 0 - Asynchronous Clock Source Enable
ADCLK_ADIV	bits 5-6 - ADC Clock Prescaler
ADCLK_MODE	bits 2-3 - 10- or 8-Bit or External-Triggered Mode Selection

MMIIC Multi-Master IIC Master Control Register (0x0040) MIMCR

MIMCR_MMALIF	bit 7 - Multi-Master Arbitration Lost Interrupt Flag
MIMCR_MMNAKIF	bit 6 - No Acknowledge Interrupt Flag
MIMCR_MMBB	bit 5 - Bus Busy Flag
MIMCR_MMAST	bit 4 - Master Control Bit
MIMCR_MMRW	bit 3 - Master Read/Write
MIMCR_MMBR2	bit 2 - Baud Rate Select Bit 2
MIMCR_MMBR1	bit 1 - Baud Rate Select Bit 1
MIMCR_MMBR0	bit 0 - Baud Rate Select Bit 0
MIMCR_MMBR	bits 0-2 - Baud Rate Select

MMIIC Multi-Master IIC Address Register (0x0041) MMADR

MMADR_MMAD7	bit 7 - Multi-Master Address Bit 7
MMADR_MMAD6	bit 6 - Multi-Master Address Bit 6
MMADR_MMAD5	bit 5 - Multi-Master Address Bit 5
MMADR_MMAD4	bit 4 - Multi-Master Address Bit 4
MMADR_MMAD3	bit 3 - Multi-Master Address Bit 3
MMADR_MMAD2	bit 2 - Multi-Master Address Bit 2
MMADR_MMAD1	bit 1 - Multi-Master Address Bit 1
MMADR_MMEXTAD	bit 0 - Multi-Master Expanded Address
MMADR_MMAD	bits 1-7 - Multi-Master Address

MMIIC Multi-Master IIC Control Register (0x0042) MMCR

MMCR_MMEN	bit 7 - Multi-Master IIC Enable
MMCR_MMIEN	bit 6 - Multi-Master IIC Interrupt Enable
MMCR_MMTXAK	bit 3 - Transmit Acknowledge Enable
MMCR_REPSEN	bit 2 - Repeated Start Enable

MMIIC Multi-Master IIC Status Register (0x0043) MMSR

MMSR_MMRXIF	bit 7 - Multi-Master IIC Receive Interrupt Flag
MMSR_MMTXIF	bit 6 - Multi-Master Transmit Interrupt Flag
MMSR_MMATCH	bit 5 - Multi-Master Address Match
MMSR_MMSRW	bit 4 - Multi-Master Slave Read/Write
MMSR_MMRXAK	bit 3 - Multi-Master Receive Acknowledge
MMSR_MMTXBE	bit 1 - Multi-Master Transmit Buffer Empty
MMSR_MMRXBF	bit 0 - Multi-Master Receive Buffer Full

MMIIC Multi-Master IIC Data Transmit Register (0x0044) MMDTR
MMDTR_MMTD7 bit 7 - Data Bit 7
MMDTR_MMTD6 bit 6 - Data Bit 6
MMDTR_MMTD5 bit 5 - Data Bit 5
MMDTR_MMTD4 bit 4 - Data Bit 4
MMDTR_MMTD3 bit 3 - Data Bit 3
MMDTR_MMTD2 bit 2 - Data Bit 2
MMDTR_MMTD1 bit 1 - Data Bit 1
MMDTR_MMTD0 bit 0 - Data Bit 0

MMIIC Multi-Master IIC Data Receive Register (0x0045) MMDRR
MMDRR_MMRD7 bit 7 - Data Bit 7
MMDRR_MMRD6 bit 6 - Data Bit 6
MMDRR_MMRD5 bit 5 - Data Bit 5
MMDRR_MMRD4 bit 4 - Data Bit 4
MMDRR_MMRD3 bit 3 - Data Bit 3
MMDRR_MMRD2 bit 2 - Data Bit 2
MMDRR_MMRD1 bit 1 - Data Bit 1
MMDRR_MMRD0 bit 0 - Data Bit 0